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EXAMINER	
KING, JUSTIN	

ART UNIT	PAPER NUMBER
2111	6

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/826,271	HOERLER ET AL.	
	Examiner	Art Unit	
	Justin I. King	2111	

-- The MAILING DATE of this communicati n appears on the cover sh et with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 January 2004* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

2. Claims 1, 7, 11, and 19-21 are rejected under 35 U.S.C. 102(a) as being anticipated by Greim et al. (U.S. Patent No. 6,163,829).

Referring to claim 1: Greim discloses an external device (figure 6, structure 134 and the attached device from path 130) coupled to a high latency path (figure 6, structure 176), the external device generating a pulsed interrupt signal for each type of interrupt supported by the processor (figure 6, structure 20); an interrupt multiplexing device (figure 6, the combined structures 120, 124, and 142) accessible by the processor over a fast bus (figure 6, structure INT4), the interrupt multiplexing device adapted to issue the interrupt to the processor in response to each pulsed interrupt signal generated by the external device (column 28, lines 20-21); a low latency path (figure 6, structure 126) coupling the external device to the interrupt multiplexing device and adapted to transport each pulsed interrupt signal generated by the external device to the interrupt multiplexing device; and a status bit (figure 6, structure 142) stored within the interrupt multiplexing device, the status bit adapted for assertion whenever the pulsed interrupt signal is detected at the interrupt multiplexing device, wherein the processor

efficiently acknowledges the issued interrupt by accessing the interrupt multiplexing device over the fast bus. Hence, claim is anticipated by the Greim.

Referring to claim 7: Greim's disclosure is stated above; furthermore, Greim discloses the DMA as the interrupt source (column 24, line 45).

Referring to claim 11: Greim discloses generating a pulsed interrupt signal at an external device (figure 6, structure 134 and the attached device from path 130) coupled to a high latency a path (figure 6, structure 176); transporting the pulsed interrupt signal to an interrupt multiplexing device (figure 6, the combined structures 120, 124, and 142) over a low latency path (figure 6, structure 126) coupling the external device to the interrupt multiplexing device; asserting a status bit (figure 6, structure 142) in response to detecting the pulsed interrupt signal at the interrupt multiplexing device; issuing the interrupt to the processor in response to each pulsed interrupt signal received at the interrupt multiplexing device (column 28, lines 20-21); and invoking an interrupt handler to service the issued interrupt. Hence, claim is anticipated by the Greim.

Referring to claim 19: Greim discloses means for generating a pulsed interrupt signal at an external device (figure 6, structure 134 and the attached device from path 130) coupled to a high latency path (figure 6, structure 176); means for transporting the pulsed interrupt signal to an interrupt multiplexing device (figure 6, the combined structures 120, 124, and 142) over a low latency path (figure 6, structure 126) coupling the external device to the interrupt multiplexing device; a means for asserting a status bit (figure 6, structure 142) in response to detecting the pulsed interrupt signal at the interrupt multiplexing device; means for issuing the interrupt to the processor in response to each pulsed interrupt signal received at the interrupt multiplexing device

(column 28, lines 20-21); and means for invoking an interrupt handler to service the issued interrupt. Hence, claim is anticipated by the Greim.

Referring to claim 20: Greim discloses generating a pulsed interrupt signal at an external device (figure 6, structure 134 and the attached device from path 130) coupled to a high latency path (figure 6, structure 176); transporting the pulsed interrupt signal to an interrupt multiplexing device (figure 6, the combined structures 120, 124, and 142) over a s low latency path (figure 6, structure 126) coupling the external device to the interrupt multiplexing device; asserting a status bit (figure 6, structure 142) in response to detecting the pulsed interrupt signal at the interrupt multiplexing device; issuing the interrupt to the processor in response to each pulsed interrupt signal received at the interrupt multiplexing device (column 28, lines 20-21); and invoking an interrupt handler to service the issued interrupt. Hence, claim is anticipated by the Greim.

Referring to claim 21: Greim discloses generating a pulsed interrupt signal at an external device (figure 6, structure 134 and the attached device from path 130) coupled to a high latency path (figure 6, structure 176), transporting the pulsed interrupt signal to an interrupt multiplexing device (figure 6, the combined structures 120, 124, and 142) over a low latency path (figure 6, structure 126) coupling the external device to the interrupt multiplexing device; asserting a status bit (figure 6, structure 142) in response to detecting the pulsed interrupt signal at the interrupt multiplexing device; issuing the interrupt to the processor in response to each pulsed interrupt signal received at the interrupt multiplexing device; and invoking an interrupt handler to service the interrupt (abstract). Hence, claim is anticipated by Greim.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. Claims 2-6 and 12-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of the Greim and Shek et al. (U.S. Patent No. 6,185,652).

Referring to claim 2: Greim's disclosure is stated above, but Greim does not explicitly disclose a current counter associated with the interrupt multiplexing device, the current counter incremented in response to each pulsed interrupt signal at the interrupt multiplexing device. Shek discloses a counter with the interrupt generator for counting the interrupt (abstract). Hence, it would have been obvious to one having ordinary skill in the computer art at the time Applicant made the invention to adapt Shek's interrupt counter to Greim because Shek teaches one how to reduce the impact on the CPU power of maintaining an interrupt counter in the CPU (column 3, lines 51-52).

Referring to claim 3: An Official Notice is taken on the following: the interrupt handler invoked by the processor to service the issued interrupt is a well-known step in every interrupt process and is disclosed in the Application as the prior art, and Applicant has not contested on this Official Notice in the response dated 1/5/04.

Referring to claim 4: Shek discloses a last counter associated with the processor, the last counter incremented in response to each interrupt serviced by the CPU (column 4, lines 20-22, the count of tasks, column 4, lines 50-53, current count, task count, and current register).

Referring to claim 5: Shek discloses comparing a value of the last counter with a value of the current counter to determine whether there are more interrupts to service (column 4, lines 38-47).

Referring to claim 6: Greim's disclosure is stated above; furthermore, Greim discloses the DMA as the interrupt source (column 24, line 45).

Referring to claim 12: Shek discloses that it is known to initialize the counter (column 12, lines 29-30).

Referring to claim 13; Greim discloses reading the status bit; and if the status bit is clear, dismissing the handler (figure 8).

Referring to claim 14: Greim discloses clearing the status bit (figure 9).

Referring to claim 15: Shek discloses if the status bit is set, reading a value of a current counter; comparing the current counter value with a value of the last counter; and if the last counter value is greater than or equal to the current counter value, returning to the step of reading the status bit (column 4, lines 38-47). Shek discloses a last counter associated with the processor, the last counter incremented in response to each interrupt serviced by the CPU

(column 4, lines 20-22, the count of tasks, column 4, lines 50-53, current count, task count, and current register).

Referring to claim 16: The admitted prior art discloses that determining whether the processor owns the control block is a part of well-known interrupt process.

Referring to claim 17: The admitted prior art discloses that it is a common-known interrupt process that when the processor owns the control block, it will process the control block. Shek discloses that it is known to increment the counter when completing the interrupt (column 6, lines 55-57).

6. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of the Greim, Shek, and Ecclesine (U.S. Patent No. 5,983,275).

Referring to claim 18: Neither Greim nor Shek explicitly discloses determining whether a preset limit for processing control blocks has been reached; and if the preset limit is reached, dismissing the handler. Ecclesine discloses that it is known to determine whether a preset limit for processing control blocks has been reached for dismissing the handler (claim 38). Hence, it would have been obvious to one having ordinary skill in the computer art at the time Applicant made the invention to adapt Ecclesine's teaching to Greim and Shek because Ecclesine teaches one to set a limit in distributing the interrupt handling processing power.

7. Claims 8-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of the Greim and design choice.

Referring to claims 8-10: Greim's disclosure is stated above; although Greim does not explicitly disclose the printed circuit board trace, PCI, or FPGA as claimed, such limitation are merely a matter of design choice and would have been obvious. The prior art teaches a direct communication between the CPU and the interrupt requester via an interrupt generator. The limitations in claims 8-10 do not define a patentably distinct invention over that in prior arts since both the invention as a whole and combined prior arts are directed to direct interrupt communication mechanism. The selection of the bus protocol, hardware bus structure, or ways to implement the interrupt generator are inconsequential for the invention as a whole and presents no new or unexpected results, so long as the direct communication between the interrupt requestor and CPU is established via the interrupt generator. Therefore, to have FPGA, PCI, or printed circuit board trace as claimed would have been a matter of obvious design choice to one of ordinary skill in the computer art. Hence, it would have been obvious to one having ordinary skill in the computer art at the time Applicant made the invention to adapt the commonly practiced PCI, FPGA, and printed circuit board trace in Greim because they are the design choice.

8. Claims 1, 7, and 19-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Swanstrom (U.S. Patent No. 5,754,884) in view of the Greim.

Referring to claim 1: Swanstrom discloses generating an interrupt signal at an external device (figure 1, structures 150 and 140), transporting the interrupt signal to an interrupt multiplexing device (figure 1, structure 160) over a first low latency path (figure 1, structures 142 and 152) that couples the external device to the interrupt multiplexing device, issuing the

interrupt to the processor over a second low latency path (figure 1, structure 112). Swanstrom discloses a status register (figure 8, structure 812), but Swanstrom does not disclose that the register is within interrupt multiplexing device. Swanstrom also does not explicitly disclose asserting a status bit in the interrupt multiplexing device corresponding to the interrupt in response to detecting the interrupt signal and reading the status bit over the second low latency path by an interrupt handler internal to the processor; clearing the status bit in response to the reading of the status bit to effectively acknowledge the interrupt. Swanstrom further does not disclose that the interrupt is a pulsed interrupt.

Greim discloses a status bit (figure 6, structure 142) stored within the interrupt multiplexing device (figure 6, structures 120, 124, and 142), the status bit adapted for assertion whenever the pulsed interrupt signal is detected at the interrupt multiplexing device, wherein the processor efficiently acknowledges the issued interrupt by accessing the interrupt multiplexing device (abstract). Grem further discloses the edge sensitive interrupt (column 22, lines 35-36), which is the pulsed interrupt.

Hence, it would have been obvious to one having ordinary skill in the computer art at the time Applicant made the invention to adapt the Greim's teaching to Swanstrom because Greim teaches one how to reduce the impact on the processor and requestor's power by maintaining an status in the processor and requestor.

Referring to claim 7: claim 1's argument applies; furthermore, Swanstrom discloses a DMA controller (figure 1, structure 150, figure 7, structure 750).

Referring to claim 19: Swanstrom discloses generating an interrupt signal at an external device (figure 1, structures 150 and 140), transporting the interrupt signal to an interrupt multiplexing

device (figure 1, structure 160) over a first low latency path (figure 1, structures 142 and 152) that couples the external device to the interrupt multiplexing device, issuing the interrupt to the processor over a second low latency path (figure 1, structure 112). Swanstrom discloses a status register (figure 8, structure 812), but Swanstrom does not disclose that the register is within interrupt multiplexing device. Swanstrom also does not explicitly disclose asserting a status bit in the interrupt multiplexing device corresponding to the interrupt in response to detecting the interrupt signal and reading the status bit over the second low latency path by an interrupt handler internal to the processor; clearing the status bit in response to the reading of the status bit to effectively acknowledge the interrupt. Swanstrom further does not disclose that the interrupt is a pulsed interrupt.

Greim discloses a status bit (figure 6, structure 142) stored within the interrupt multiplexing device (figure 6, structures 120, 124, and 142), the status bit adapted for assertion whenever the pulsed interrupt signal is detected at the interrupt multiplexing device, wherein the processor efficiently acknowledges the issued interrupt by accessing the interrupt multiplexing device (abstract). Grem further discloses the edge sensitive interrupt (column 22, lines 35-36), which is the pulsed interrupt.

Hence, it would have been obvious to one having ordinary skill in the computer art at the time Applicant made the invention to adapt the Greim's teaching to Swanstrom because Greim teaches one how to reduce the impact on the processor and requestor's power by maintaining an status in the processor and requestor.

Referring to claim 20: Swanstrom discloses generating an interrupt signal at an external device (figure 1, structures 150 and 140), transporting the interrupt signal to an interrupt

multiplexing device (figure 1, structure 160) over a first low latency path (figure 1, structures 142 and 152) that couples the external device to the interrupt multiplexing device, issuing the interrupt to the processor over a second low latency path (figure 1, structure 112). Swanstrom discloses a status register (figure 8, structure 812), but Swanstrom does not disclose that the register is within interrupt multiplexing device. Swanstrom also does not explicitly disclose asserting a status bit in the interrupt multiplexing device corresponding to the interrupt in response to detecting the interrupt signal and reading the status bit over the second low latency path by an interrupt handler internal to the processor; clearing the status bit in response to the reading of the status bit to effectively acknowledge the interrupt. Swanstrom further does not disclose that the interrupt is a pulsed interrupt.

Greim discloses a status bit (figure 6, structure 142) stored within the interrupt multiplexing device (figure 6, structures 120, 124, and 142), the status bit adapted for assertion whenever the pulsed interrupt signal is detected at the interrupt multiplexing device, wherein the processor efficiently acknowledges the issued interrupt by accessing the interrupt multiplexing device (abstract). Grem further discloses the edge sensitive interrupt (column 22, lines 35-36), which is the pulsed interrupt.

Hence, it would have been obvious to one having ordinary skill in the computer art at the time Applicant made the invention to adapt the Greim's teaching to Swanstrom because Greim teaches one how to reduce the impact on the processor and requestor's power by maintaining an status in the processor and requestor.

Referring to claim 21: Swanstrom discloses generating an interrupt signal at an external device (figure 1, structures 150 and 140), transporting the interrupt signal to an interrupt

multiplexing device (figure 1, structure 160) over a first low latency path (figure 1, structures 142 and 152) that couples the external device to the interrupt multiplexing device, issuing the interrupt to the processor over a second low latency path (figure 1, structure 112). Swanstrom discloses a status register (figure 8, structure 812), but Swanstrom does not disclose that the register is within interrupt multiplexing device. Swanstrom also does not explicitly disclose asserting a status bit in the interrupt multiplexing device corresponding to the interrupt in response to detecting the interrupt signal and reading the status bit over the second low latency path by an interrupt handler internal to the processor; clearing the status bit in response to the reading of the status bit to effectively acknowledge the interrupt. Swanstrom further does not disclose that the interrupt is a pulsed interrupt.

Greim discloses a status bit (figure 6, structure 142) stored within the interrupt multiplexing device (figure 6, structures 120, 124, and 142), the status bit adapted for assertion whenever the pulsed interrupt signal is detected at the interrupt multiplexing device, wherein the processor efficiently acknowledges the issued interrupt by accessing the interrupt multiplexing device (abstract). Greim further discloses the edge sensitive interrupt (column 22, lines 35-36), which is the pulsed interrupt.

Hence, it would have been obvious to one having ordinary skill in the computer art at the time Applicant made the invention to adapt the Greim's teaching to Swanstrom because Greim teaches one how to reduce the impact on the processor and requestor's power by maintaining an status in the processor and requestor.

9. Claims 2-6 and 12-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Swanstrom in view of the Greim and Shek.

Referring to claim 2: Neither Swanstrom nor Greim explicitly disclose a current counter associated with the interrupt multiplexing device, the current counter incremented in response to each pulsed interrupt signal at the interrupt multiplexing device. Shek discloses a counter with the interrupt generator for counting the interrupt (abstract). Hence, it would have been obvious to one having ordinary skill in the computer art at the time Applicant made the invention to adapt Shek's interrupt counter to Greim because Shek teaches one how to reduce the impact on the CPU power of maintaining an interrupt counter in the CPU (column 3, lines 51-52).

Referring to claim 3: The interrupt handler invoked by the processor to service the issued interrupt is a well-known step in every interrupt process and is disclosed in the Application as the prior art.

Referring to claim 4: Shek discloses a last counter associated with the processor, the last counter incremented in response to each interrupt serviced by the CPU (column 4, lines 20-22, the count of tasks, column 4, lines 50-53, current count, task count, and current register).

Referring to claim 5: Shek discloses comparing a value of the last counter with a value of the current counter to determine whether there are more interrupts to service (column 4, lines 38-47).

Referring to claim 6: Greim's disclosure is stated above; furthermore, Greim discloses the DMA as the interrupt source (column 24, line 45).

Referring to claim 12: Shek discloses that it is known to initialize the counter (column 12, lines 29-30) and Shek discloses a last counter associated with the processor, the last counter

incremented in response to each interrupt serviced by the CPU (column 4, lines 20-22, the count of tasks, column 4, lines 50-53, current count, task count, and current register).

Referring to claim 13; Greim discloses reading the status bit; and if the status bit is clear, dismissing the handler (figure 8).

Referring to claim 14: Greim discloses clearing the status bit (figure 9).

Referring to claim 15: Shek discloses if the status bit is set, reading a value of a current counter; comparing the current counter value with a value of the last counter; and if the last counter value is greater than or equal to the current counter value, returning to the step of reading the status bit (column 4, lines 38-47). Shek discloses a last counter associated with the processor, the last counter incremented in response to each interrupt serviced by the CPU (column 4, lines 20-22, the count of tasks, column 4, lines 50-53, current count, task count, and current register).

Referring to claim 16: The admitted prior art discloses that determining whether the processor owns the control block is a part of well-known interrupt process.

Referring to claim 17: The admitted prior art discloses that it is a common-known interrupt process that when the processor owns the control block, it will process the control block. Shek discloses that it is known to increment the counter when completing the interrupt (column 6, lines 55-57).

10. Claims 8-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of the Swanstrom, Greim and design choice.

Referring to claims 8-10: Although prior arts do not explicitly disclose the printed circuit board trace, PCI, or FPGA as claimed, such limitation are merely a matter of design choice and would have been obvious. The prior art teaches a direct communication between the CPU and the interrupt requester via an interrupt generator. The limitations in claims 8-10 do not define a patentably distinct invention over that in prior arts since both the invention as a whole and combined prior arts are directed to direct interrupt communication mechanism. The selection of the bus protocol, hardware bus structure, or ways to implement the interrupt generator are inconsequential for the invention as a whole and presents no new or unexpected results, so long as the direct communication between the interrupt requestor and CPU is established via the interrupt generator. Therefore, to have FPGA, PCI, or printed circuit board trace as claimed would have been a matter of obvious design choice to one of ordinary skill in the computer art. Hence, it would have been obvious to one having ordinary skill in the computer art at the time Applicant made the invention to adapt the commonly practiced PCI, FPGA, and printed circuit board trace in Swanstrom and Greim because they are the design choice.

11. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of the Swanstrom, Greim, Shek, and Ecclesine.

Referring to claim 18: Neither Greim nor Shek explicitly discloses determining whether a preset limit for processing control blocks has been reached; and if the preset limit is reached, dismissing the handler. Ecclesine discloses that it is known to determine whether a preset limit for processing control blocks has been reached for dismissing the handler (claim 38). Hence, it would have been obvious to one having ordinary skill in the computer art at the time Applicant

made the invention to adapt Ecclesine's teaching to Swanstrom, Greim, and Shek because Ecclesine teaches one to set a limit in distributing the interrupt handling processing power.

12. Claims 22-24, 27-29, and 32-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Swanstrom in view of the Greim and Okbay et al. (U.S. Patent No. 6,606,677).

Referring to claim 22: Swanstrom discloses generating an interrupt signal at an external device (figure 1, structures 150 and 140), transporting the interrupt signal to an interrupt multiplexing device (figure 1, structure 160) over a first low latency path (figure 1, structures 142 and 152) that couples the external device to the interrupt multiplexing device, issuing the interrupt to the processor over a second low latency path (figure 1, structure 112). Swanstrom discloses a status register (figure 8, structure 812), but Swanstrom does not disclose that the register is within interrupt multiplexing device. Swanstrom also does not explicitly disclose asserting a status bit in the interrupt multiplexing device corresponding to the interrupt in response to detecting the interrupt signal and reading the status bit over the second low latency path by an interrupt handler internal to the processor; clearing the status bit in response to the reading of the status bit to effectively acknowledge the interrupt. Swanstrom further does not disclose that the interrupt is a pulsed interrupt.

Greim discloses a status bit (figure 6, structure 142) stored within the interrupt multiplexing device (figure 6, structures 120, 124, and 142), the status bit adapted for assertion whenever the pulsed interrupt signal is detected at the interrupt multiplexing device, wherein the processor efficiently acknowledges the issued interrupt by accessing the interrupt multiplexing

device (abstract). Greim further discloses the edge sensitive interrupt (column 22, lines 35-36), which is the pulsed interrupt.

Neither Swanstrom nor Greim discloses that the interrupt handler is within the processor. Okbay discloses that it is known to integrate the interrupt handler within the processor to improve the interrupt handling (figure 3, structure 314).

Hence, it would have been obvious to one having ordinary skill in the computer art at the time Applicant made the invention to adapt the Greim and Okbay's teachings to Swanstrom because Greim teaches one how to reduce the impact on the processor and requestor's power by maintaining an status in the processor and requestor and Okbay teaches one to expedite the interrupt handling by integrating the interrupt handler within the processor.

Referring to claim 23: The admitted prior art discloses that determining whether the processor owns the control block and processing the control block are a part of well-known interrupt process.

Referring to claim 24: When the interrupt is completed and return back to the requester on the high latency path, it is the assigning ownership of the control block over a high latency path.

Referring to claim 27: Swanstrom discloses generating an interrupt signal at an external device (figure 1, structures 150 and 140), transporting the interrupt signal to an interrupt multiplexing device (figure 1, structure 160) over a first low latency path (figure 1, structures 142 and 152) that couples the external device to the interrupt multiplexing device, issuing the interrupt to the processor over a second low latency path (figure 1, structure 112). Swanstrom discloses a status register (figure 8, structure 812), but Swanstrom does not disclose that the

register is within interrupt multiplexing device. Swanstrom also does not explicitly disclose asserting a status bit in the interrupt multiplexing device corresponding to the interrupt in response to detecting the interrupt signal and reading the status bit over the second low latency path by an interrupt handler internal to the processor; clearing the status bit in response to the reading of the status bit to effectively acknowledge the interrupt. Swanstrom further does not disclose that the interrupt is a pulsed interrupt.

Greim discloses a status bit (figure 6, structure 142) stored within the interrupt multiplexing device (figure 6, structures 120, 124, and 142), the status bit adapted for assertion whenever the pulsed interrupt signal is detected at the interrupt multiplexing device, wherein the processor efficiently acknowledges the issued interrupt by accessing the interrupt multiplexing device (abstract). Grem further discloses the edge sensitive interrupt (column 22, lines 35-36), which is the pulsed interrupt.

Neither Swanstrom nor Greim discloses that the interrupt handler is within the processor. Okbay discloses that it is known to integrate the interrupt handler within the processor to improve the interrupt handling (figure 3, structure 314).

Hence, it would have been obvious to one having ordinary skill in the computer art at the time Applicant made the invention to adapt the Greim and Okbay's teachings to Swanstrom because Greim teaches one how to reduce the impact on the processor and requestor's power by maintaining an status in the processor and requestor and Okbay teaches one to expedite the interrupt handling by integrating the interrupt handler within the processor.

Referring to claim 28: The admitted prior art discloses that determining whether the processor owns the control block and processing the control block are a part of well-known interrupt process.

Referring to claim 29: When the interrupt is completed and return back to the requester on the high latency path, it is the assigning ownership of the control block over a high latency path.

Referring to claim 32: Swanstrom discloses generating an interrupt signal at an external device (figure 1, structures 150 and 140), transporting the interrupt signal to an interrupt multiplexing device (figure 1, structure 160) over a first low latency path (figure 1, structures 142 and 152) that couples the external device to the interrupt multiplexing device, issuing the interrupt to the processor over a second low latency path (figure 1, structure 112). Swanstrom discloses a status register (figure 8, structure 812), but Swanstrom does not disclose that the register is within interrupt multiplexing device. Swanstrom also does not explicitly disclose asserting a status bit in the interrupt multiplexing device corresponding to the interrupt in response to detecting the interrupt signal and reading the status bit over the second low latency path by an interrupt handler internal to the processor; clearing the status bit in response to the reading of the status bit to effectively acknowledge the interrupt. Swanstrom further does not disclose that the interrupt is a pulsed interrupt.

Greim discloses a status bit (figure 6, structure 142) stored within the interrupt multiplexing device (figure 6, structures 120, 124, and 142), the status bit adapted for assertion whenever the pulsed interrupt signal is detected at the interrupt multiplexing device, wherein the processor efficiently acknowledges the issued interrupt by accessing the interrupt multiplexing

device (abstract). Greim further discloses the edge sensitive interrupt (column 22, lines 35-36), which is the pulsed interrupt.

Neither Swanstrom nor Greim discloses that the interrupt handler is within the processor. Okbay discloses that it is known to integrate the interrupt handler within the processor to improve the interrupt handling (figure 3, structure 314).

Hence, it would have been obvious to one having ordinary skill in the computer art at the time Applicant made the invention to adapt the Greim and Okbay's teachings to Swanstrom because Greim teaches one how to reduce the impact on the processor and requestor's power by maintaining an status in the processor and requestor and Okbay teaches one to expedite the interrupt handling by integrating the interrupt handler within the processor.

Referring to claim 33: Swanstrom discloses generating an interrupt signal at an external device (figure 1, structures 150 and 140), transporting the interrupt signal to an interrupt multiplexing device (figure 1, structure 160) over a first low latency path (figure 1, structures 142 and 152) that couples the external device to the interrupt multiplexing device, issuing the interrupt to the processor over a second low latency path (figure 1, structure 112). Swanstrom discloses a status register (figure 8, structure 812), but Swanstrom does not disclose that the register is within interrupt multiplexing device. Swanstrom also does not explicitly disclose asserting a status bit in the interrupt multiplexing device corresponding to the interrupt in response to detecting the interrupt signal and reading the status bit over the second low latency path by an interrupt handler internal to the processor; clearing the status bit in response to the reading of the status bit to effectively acknowledge the interrupt. Swanstrom further does not disclose that the interrupt is a pulsed interrupt.

Greim discloses a status bit (figure 6, structure 142) stored within the interrupt multiplexing device (figure 6, structures 120, 124, and 142), the status bit adapted for assertion whenever the pulsed interrupt signal is detected at the interrupt multiplexing device, wherein the processor efficiently acknowledges the issued interrupt by accessing the interrupt multiplexing device (abstract). Grem further discloses the edge sensitive interrupt (column 22, lines 35-36), which is the pulsed interrupt.

Neither Swanstrom nor Greim discloses that the interrupt handler is within the processor. Okbay discloses that it is known to integrate the interrupt handler within the processor to improve the interrupt handling (figure 3, structure 314).

Hence, it would have been obvious to one having ordinary skill in the computer art at the time Applicant made the invention to adapt the Greim and Okbay's teachings to Swanstrom because Greim teaches one how to reduce the impact on the processor and requestor's power by maintaining an status in the processor and requestor and Okbay teaches one to expedite the interrupt handling by integrating the interrupt handler within the processor.

Referring to claim 34: Swanstrom discloses generating an interrupt signal at an external device (figure 1, structures 150 and 140), transporting the interrupt signal to an interrupt multiplexing device (figure 1, structure 160) over a first low latency path (figure 1, structures 142 and 152) that couples the external device to the interrupt multiplexing device, issuing the interrupt to the processor over a second low latency path (figure 1, structure 112). Swanstrom discloses a status register (figure 8, structure 812), but Swanstrom does not disclose that the register is within interrupt multiplexing device. Swanstrom also does not explicitly disclose asserting a status bit in the interrupt multiplexing device corresponding to the interrupt in

response to detecting the interrupt signal and reading the status bit over the second low latency path by an interrupt handler internal to the processor; clearing the status bit in response to the reading of the status bit to effectively acknowledge the interrupt. Swanstrom further does not disclose that the interrupt is a pulsed interrupt.

Greim discloses a status bit (figure 6, structure 142) stored within the interrupt multiplexing device (figure 6, structures 120, 124, and 142), the status bit adapted for assertion whenever the pulsed interrupt signal is detected at the interrupt multiplexing device, wherein the processor efficiently acknowledges the issued interrupt by accessing the interrupt multiplexing device (abstract). Grem further discloses the edge sensitive interrupt (column 22, lines 35-36), which is the pulsed interrupt.

Neither Swanstrom nor Greim discloses that the interrupt handler is within the processor. Okbay discloses that it is known to integrate the interrupt handler within the processor to improve the interrupt handling (figure 3, structure 314).

Hence, it would have been obvious to one having ordinary skill in the computer art at the time Applicant made the invention to adapt the Greim and Okbay's teachings to Swanstrom because Greim teaches one how to reduce the impact on the processor and requestor's power by maintaining an status in the processor and requestor and Okbay teaches one to expedite the interrupt handling by integrating the interrupt handler within the processor.

13. Claims 25 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Swanstrom in view of the Greim, Okbay, and Shek.

Referring to claims 25 and 30: The disclosures of Swanstrom, Greim, and Okbay are stated above. None of them explicitly discloses a current counter associated with the interrupt multiplexing device, the current counter incremented in response to each pulsed interrupt signal at the interrupt multiplexing device. Shek discloses a counter with the interrupt generator for counting the interrupt (abstract). Shek further discloses a last counter associated with the processor, the last counter incremented in response to each interrupt serviced by the CPU (column 4, lines 20-22, the count of tasks, column 4, lines 50-53, current count, task count, and current register). Shek also discloses comparing a value of the last counter with a value of the current counter to determine whether there are more interrupts to service (column 4, lines 38-47).

Hence, it would have been obvious to one having ordinary skill in the computer art at the time Applicant made the invention to adapt Shek's interrupt counter to Swanstrom, Greim, and Okbay because Shek teaches one how to reduce the impact on the CPU power of maintaining an interrupt counter in the CPU (column 3, lines 51-52).

14. Claim 26 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of the Swanstrom, Greim, Okbay, Shek, and Ecclesine.

Referring to claim 26 and 31: None of Swanstrom, Greim, Okbay, and Shek explicitly discloses determining whether a preset limit for processing control blocks has been reached; and if the preset limit is reached, dismissing the handler. Ecclesine discloses that it is known to determine whether a preset limit for processing control blocks has been reached for dismissing the handler (claim 38). Hence, it would have been obvious to one having ordinary skill in the computer art at the time Applicant made the invention to adapt Ecclesine's teaching to

Swanstrom, Greim, Okbay, and Shek because Ecclesine teaches one to set a limit in distributing the interrupt handling processing power.

Response to Arguments

15. In response to Applicant's argument that the prior art on record does not disclose "the external device generating a *pulsed* interrupt signal for each type of interrupt supported by the processor" and "the interrupt multiplexing device adapted to issue the interrupt to the processor in response to each *pulsed* interrupt signal generated by the external device" (Remark, page 16, 2nd paragraph): Greim does disclose the pulsed interrupt. Greim discloses that the interrupts are edge sensitive (column 22, lines 34-35). The edge sensitive interrupt (raising edge or falling edge) is the pulsed interrupt. Greim's structure 134 and the attached device from path 130 in the figure 6 is the claimed external device, which generates the interrupt, and a multiplexing device (figure 6, structure 120) adapted to issue the interrupt to the processor.

Conclusion

16. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

17. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Justin King whose telephone number is (703) 305-4571. The examiner can normally be reached on Monday through Friday from 9:00 A.M. to 5:00 P.M..

If attempts to reach the examiner by telephones are unsuccessfully, the examiner's supervisor, Mark Reinhart can be reached at (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose number is (703)-306-5631.

Justin King
March 16, 2004

Gopal C. Ray
GOPAL C. RAY
PRIMARY EXAMINER
GROUP 2100